Amendments to the Specification:

The Paragraph beginning at Page 18, lines 1 - 25, is to be amended as follows:

Figure 389 shows a high level block diagram of QA Chip
Figure 390 shows an analogue unit
Figure 391 shows a serial bus protocol for trimming
Figure 392 shows a block diagram of a trim unit
Figure 393 shows a block diagram of a CPU of the QA chip
Figure 394 shows block diagram of an MIU
Figure 395 shows a block diagram of memory components
Figure 396 shows a first byte sent to an IOU
Figure 397 shows a block diagram of the IOU
Figure 398 shows a relationship between external SDa and SClk and generation of internal signals
Figure 399 shows block diagram of ALU
Figure 400 shows a block diagram of DataSel
Figure 401 shows a block diagram of ROR
Figure 402 shows a block diagram of the ALU's IO block
Figure 403 shows a block diagram of PCU
Figure 404 shows a block diagram of an Address Generator Unit
Figure 405 shows a block diagram for a Counter Unit
Figure 406 shows a block diagram of PMU
Figure 407 shows a state machine for PMU
Figure 408 shows a block diagram of MRU
Figure 409 shows simplified MAU state machine
Figure 410 shows power-on reset behaviour
Figure 411 shows a ring oscillator block diagram
Figure 412 shows a system clock duty cycle
~~Figure 413 shows power-on reset~~